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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,679	LIN, FENG	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/09/03,02/19/04*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 50 are presented for examination.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 41 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In the claim 41, the claimed "one circuit" in line 2, and "one circuit" in line 3 on page 15, examiner is not clear that both are same or different circuits, however examiner proceeds with both as different circuits.

3. Claim 46 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In the claim 41, the claimed "one circuit" in line 4, and "one circuit" in line 5 on page 16, examiner is not clear that both are same or different circuits, however examiner proceeds with both as different circuits.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 – 10, and 41 – 42 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Baker et al. [hereinafter as Baker], US Patent 6, 445, 231 [cited by applicant in IDS paper filed on 02/19/04].

6. As to claim 1, Baker discloses a locked loop [DLL] comprising:

a. a delay line [111, delayed locked loop] having a first [205a, coarse loop delay] portion providing a variable amount of delay [wide frequency range] substantially independent of process, temperature, and voltage variations [PVT changes] [it is inherent property to wide frequency range which do not vary with PVT changes] and a second [205b, fine loop delay] portion in series with said first portion [205a in series with 205b, fig. 2A, and 11] and providing a variable amount of delay [delay range] that substantially tracks [dynamically track] changes [variations] in process, temperature, and voltage [PVT] variations [process variations] [col. 4, lines 17 - 20, fig. 2A, 3A, 9, and 11];

b. a control circuit [308, shift register] for controlling the delay of said delay line [205a][col. 4, lines 60 – 65, fig. 3A, 12];

c. a phase detector [302, phase detector] for producing signals [SL, SR] for input to said control circuit [col. 4, lines 55 – 60, fig. 2A, 3A]; and

d. a feedback path [207] for connecting an output [210, CLKout]of said delay line to an input of said delay line [205a] and to said phase detector [302][col. 3, lines 66 – 67, fig.2A, 3A, and 11].

7. As to claim 2, Baker discloses the locked loop [111] with a first portion [205a, coarse loop delay which provides wide frequency range which do not vary with PVT changes] of said delay line [111] has a small intrinsic [PVT dependent] delay and said second portion [205b, fine loop delay] of said delay line has a higher intrinsic [PVT dependent] delay [it is an inherent property of PVT independent coarse loop to have a small intrinsic (PVT dependent) delay than PVT dependent fine loop][col. 4, lines 17 – 20].

8. As to claim 3, Baker discloses to vary delay of first portion [205a] of delay line [111] by varying the load [number of stages] [col. 6, lines 20 – 28] and second portion [205b] of delay line [111] by selecting a desired signal path [col. 8, lines 34 – 50, fig. 10].

9. As to claim 4, Baker discloses the desired [selected] path signal is one of a slow [longer] path and a fast [shorter] path [col. 8, lines 39 –50, fig. 10].

10. As to claim 5, Baker discloses the desired [selected] path signal is one of a series path through an inverter or a parallel path through inverter [col. 8, lines 34 – 45, fig. 10].

11. As to claim 6, Baker discloses a locked loop [DLL] comprising:

a. a delay line [111] having a first portion [205a] providing a variable amount of delay [wide frequency range] with little intrinsic [PVT dependent] delay and a second portion [205b] providing a variable amount of delay [delay range] with larger intrinsic [PVT dependent] delay [it is an inherent property of PVT independent coarse loop to have a small intrinsic (PVT dependent) delay than PVT dependent fine loop][col. 4, lines 17 – 20];

b. a control circuit [308, shift register] for controlling the delay of said delay line [205a][col. 4, lines 60 – 65, fig. 3A, 12];

c. a phase detector [302, phase detector] for producing signals [SL, SR] for input to said control circuit [col. 4, lines 55 – 60, fig. 2A, 3A]; and

d. a feedback path [207] for connecting an output [210, CLKout]of said delay line to an input of said delay line [205a] and to said phase detector [302][col. 3, lines 66 – 67, fig.2A, 3A, and 11].

12. As to claim 7, Baker teaches a delay [111, delayed locked loop] having a first [205a, coarse loop delay] portion providing a variable amount of delay [wide frequency range] substantially independent of process, temperature, and voltage variations [PVT changes] [it is inherent property to wide frequency range which do not vary with PVT changes] and a second [205b, fine loop delay] portion of delay [delay range] that substantially tracks [dynamically track] changes [variations] in process, temperature, and voltage [PVT] variations [process variations] [col. 4, lines 17 - 20, fig. 2A, 3A, 9, and 11].

13. As to claim 8, Baker discloses to vary delay of first portion [205a] of delay line [111] by varying the load [number of stages] [col. 6, lines 20 – 28] and second portion [205b] of delay line [111] by selecting a desired signal path [col. 8, lines 34 – 50, fig. 10].

14. As to claim 9, Baker discloses the desired [selected] path signal is one of a slow [longer] path and a fast [shorter] path [col. 8, lines 39 –50, fig. 10].

15. As to claim 10, Baker discloses the desired [selected] path signal is one of a series path through an inverter or a parallel path through inverter [col. 8, lines 34 – 45, fig. 10].

16. As to claim 41, Baker discloses a locked loop [DLL] comprising:

a. propagating a signal through two different [205a, 205b] types of variable delay circuits [fig. 2], one circuit [205a, coarse loop delay with wide frequency range] being

substantially independent of process, temperature, and voltage variations [PVT changes] [it is inherent property to wide frequency range which do not vary with PVT changes] and other circuit [205b, fine loop delay] tracks [dynamically track] changes [variations] in process, temperature, and voltage [PVT] variations [process variations] [col. 4, lines 17 - 20, fig. 2A, 3A, 9, and 11];

b. feeding back the propagated signal [CLKout] to the input of one of the delay circuits [205a, 205b] and a phase detector [302, [col. 3, lines 66 – 67, fig.2A, 3A, and 11];

c. detecting a phase difference [it is inherent property of phase detector] between said feedback signal [CLKout] and a reference signal [CLKout] to produce control signals [SL, SR] for delay circuit [col. 4, lines 55 – 60, fig. 2A, 3A].

17. As to claim 42, Baker discloses a locked loop [DLL] comprising:

a. propagating a signal through two different [205a, 205b] types of variable delay circuits [fig. 2], one circuit [205a] have a small intrinsic delay [coarse loop providing a variable amount of delay for wide frequency range with little intrinsic (PVT dependent) delay] and other circuit having a larger intrinsic delay [PVT dependent][it is an inherent property of PVT independent coarse loop for wide frequency range to have a small intrinsic (PVT dependent) delay than PVT dependent fine loop][col. 4, lines 17 – 20];

b. feeding back the propagated signal [CLKout] to the input of one of the delay circuits [205a, 205b] and a phase detector [302, [col. 3, lines 66 – 67, fig.2A, 3A, and 11];

c. detecting a phase difference [it is inherent property of phase detector] between said feedback signal [CLKout] and a reference signal [CLKout] to produce control signals [SL, SR] for delay circuit [col. 4, lines 55 – 60, fig. 2A, 3A].

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

19. Claims 11 – 20, 31 – 40, and 43 – 50 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ono, US Patent 5,923,715.

20. As to claim 11, Ono teaches locked loop [digital phase-locked loop] comprising:

a. a first circuit path [via load cap. Control 12, fig. 1, 2] having a stepwise variable [adder/subtracter circuit increments or decrements] capacitive load [load capacitance] [col. 4, lines 11 – 21];

b. a second circuit path [via delay stage control 13, fig. 1, 2] in series [13 in series with 12] with first circuit path and having a plurality of stages [number of delay stages] each having at least two paths [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2];

c. a control circuit [15, 13, load cap. Control, delay stage control] for controlling the amount of capacitance [load capacitance] in the first circuit path and number of stages [number of delay stages] in the second circuit path [col. 4, lines 48 – 67, col. 5, lines 1 – 14];

d. a phase detector [14, phase comparator] for producing signals for input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1]; and

e. a feedback path [F2] between an output [Digital PLL output] of second circuit path and an input of the first circuit path and to said phase detector [14][fig.1, 7].

21. As to claim 12, it is inherent to Ono's first circuit path [with increment/decrement of load capacitance] of having a smaller intrinsic delay than the second circuit path [with number of delay stages].

22. As to claim 13, it is inherent property of Ono's first circuit path [via load cap control] with phase comparator to have substantially independent of process, temperature and voltage [PVT] variations [phase variation is independent of PVT variations] while second circuit path [variable delay stage control] with frequency comparator to have substantially tracks changes in PVT [frequency variation dependent to PVT changes].

23. As to claim 14, Ono discloses two paths include a fast [with lesser delay stages]and a slow [with more delay stages] path [fig.2].

24. As to claim 15, Ono discloses two paths include a series path through an inverter [21, 22, 23,..] and a parallel path [Cn1, Cn2, …] through inverters [26 of Cn1,..][fig.2].

25. As to claim 16, Ono teaches locked loop [digital phase-locked loop] comprising:

a. a first circuit path [via load cap. Control 12, fig. 1, 2] having a stepwise variable [adder/subtracter circuit increments or decrements] capacitive load [load capacitance] [col. 4, lines 11 – 21];

b. a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least two paths [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2];

c. a control circuit [15, 13, load cap. Control, delay stage control] for controlling the amount of capacitance [load capacitance] in the first circuit path and number of stages [number of delay stages] in the second circuit path [col. 4, lines 48 – 67, col. 5, lines 1 – 14];

d. a phase detector [14, phase comparator] for producing signals for input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1]; and

e. a feedback path [F2] between an output [Digital PLL output] of second circuit path and an input of the first circuit path and to said phase detector [14][fig.1, 7].

26. As to claim 17, it is inherent to Ono's first circuit path [with increment/decrement of load capacitance] of having a smaller intrinsic delay than the second circuit path [with number of delay stages].

27. As to claim 18, it is inherent property of Ono's first circuit path [via load cap control] with phase comparator to have substantially independent of process, temperature and voltage [PVT] variations [phase variation is independent of PVT variations] while second circuit path [variable delay stage control] with frequency comparator to have substantially tracks changes in PVT [frequency variation dependent to PVT changes].

28. As to claim 19, Ono teaches locked loop [digital phase-locked loop] comprising:

a. a first circuit path [via load cap. Control 12, fig. 1, 2] having a variable amount [adder/subtracter circuit increments or decrements] of drive [load capacitance] associated therewith [col. 4, lines 11 – 21];

b. a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least a fast [with less number of delay stages] and slow [with more number of delay stages] path [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2];

c. a control circuit [15, 13, load cap. Control, delay stage control] for controlling number of stages [number of capacitive load stages] in the first circuit path and number of stages [number of delay stages] in the second circuit path [col. 4, lines 48 – 67, col. 5, lines 1 – 14];

d. a phase detector [14, phase comparator] for producing signals for input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1]; and

e. a feedback path [F2] between an output [Digital PLL output] of second circuit path and an input of the first circuit path and to said phase detector [14][fig.1, 7].

29. As to claim 20, it is inherent to Ono's first circuit path [with increment/decrement of load capacitance] of having a smaller intrinsic delay than the second circuit path [with number of delay stages].

30. As to claim 31, Ono teaches locked loop [digital phase-locked loop] comprising:

a. a first locked loop [DLL with phase comparator] to establish a phase relationship [inherent to phase comparator] between an output [F2, DPLL output clock signal] and reference signal [F1, refernce clock signal][fig. 1];

b. a second locked loop [DLL with frequency comparator] responsive to said first locked loop [DLL with phase comparator] and comprising:

c. a delay line [16, variable delay circuit] having a first circuit path [via load cap. Control 12, fig. 1, 2] having a stepwise variable [adder/subtracter circuit increments or decrements] capacitive load [load capacitance] [col. 4, lines 11 – 21];

d. a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least two paths [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2];

e. a control circuit [15, 13, load cap. Control, delay stage control] for controlling the amount of capacitance [load capacitance] in the first circuit path and number of stages [number of delay stages] in the second circuit path [col. 4, lines 48 – 67, col. 5, lines 1 – 14];

f. a phase detector [14, phase comparator] for producing signals for input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1]; and

g. a feedback path [F2] between an output [Digital PLL output] of second circuit path and an input of the first circuit path and to said phase detector [14][fig.1, 7].

31. As to claim 32, it is inherent to Ono's first circuit path [with increment/decrement of load capacitance] of having a smaller intrinsic delay than the second circuit path [with number of delay stages].

32. As to claim 33, it is inherent property of Ono's first circuit path [via load cap control] with phase comparator to have substantially independent of process, temperature and voltage [PVT] variations [phase variation is independent of PVT variations] while second circuit path [variable delay stage control] with frequency comparator to have substantially tracks changes in PVT [frequency variation dependent to PVT changes].

33. As to claim 34, Ono discloses two paths include a fast [with lesser delay stages] and a slow [with more delay stages] path [fig.2].

34. As to claim 35, Ono discloses two paths include a series path through an inverter [21, 22, 23,] and a parallel path [Cn1, Cn2,] through inverters [26 of Cn1,][fig.2].

35. As to claim 36, Ono teaches locked loop [digital phase-locked loop] comprising:

a. a first locked loop [DLL with phase comparator] to establish a phase relationship [inherent to phase comparator] between an output [F2, DPLL output clock signal] and reference signal [F1, reference clock signal][fig. 1];

b. a second locked loop [DLL with frequency comparator] responsive to said first locked loop [DLL with phase comparator] [fig.1] and comprising:

c. a delay line [16, variable delay circuit] having a first circuit path [via load cap. Control 12, fig. 1, 2] having a stepwise variable [adder/subtracter circuit increments or decrements] capacitive load [load capacitance] [col. 4, lines 11 – 21];

d. a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least two paths [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2];

e. a control circuit [15, 13, load cap. Control, delay stage control] for controlling the amount of capacitance [load capacitance] in the first circuit path and number of stages [number of delay stages] in the second circuit path [col. 4, lines 48 – 67, col. 5, lines 1 – 14];

f. a phase detector [14, phase comparator] for producing signals for input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1]; and

g. a feedback path [F2] between an output [Digital PLL output] of second circuit path and an input of the first circuit path and to said phase detector [14][fig.1, 7].

36. As to claim 37, it is inherent to Ono's first circuit path [with increment/decrement of load capacitance] of having a smaller intrinsic delay than the second circuit path [with number of delay stages].

37. As to claim 38, it is inherent property of Ono's first circuit path [via load cap control] with phase comparator to have substantially independent of process, temperature and voltage [PVT] variations [phase variation is independent of PVT variations] while second circuit path [variable delay stage control] with frequency comparator to have substantially tracks changes in PVT [frequency variation dependent to PVT changes].

38. As to claim 39, Ono teaches locked loop [digital phase-locked loop] comprising:

a. a first locked loop [DLL with phase comparator] to establish a phase relationship [inherent to phase comparator] between an output [F2, DPLL output clock signal] and reference signal [F1, reference clock signal][fig. 1];

b. a second locked loop [DLL with frequency comparator] responsive to said first locked loop [DLL with phase comparator] [fig.1] and comprising:

c. a first circuit path [via load cap. Control 12, fig. 1, 2] having a variable amount [adder/subtracter circuit increments or decrements] of drive [load capacitance] associated therewith [col. 4, lines 11 – 21];

d. a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least a fast [with less number of delay

stages] and slow [with more number of delay stages] path [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2];

e. a control circuit [15, 13, load cap. Control, delay stage control] for controlling number of stages [number of capacitive load stages] in the first circuit path and number of stages [number of delay stages] in the second circuit path [col. 4, lines 48 – 67, col. 5, lines 1 – 14];

f. a phase detector [14, phase comparator] for producing signals for input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1]; and

g. a feedback path [F2] between an output [Digital PLL output] of second circuit path and an input of the first circuit path and to said phase detector [14][fig.1, 7].

39. As to claim 40, it is inherent to Ono's first circuit path [with increment/decrement of load capacitance] of having a smaller intrinsic delay than the second circuit path [with number of delay stages].

40. As to claim 43, Ono teaches locked loop [digital phase-locked loop] comprising:

a. propagating a signal through a first circuit [14] path [via load cap. Control 12, fig. 1, 2] having a stepwise variable [adder/subtracter circuit increments or decrements] capacitive load [load capacitance] [col. 4, lines 11 – 21];

b. propagating a signal through a second [11] circuit path [via delay stage control 13, fig. 1, 2] in series [13 in series with 12] with first circuit path and having a plurality of stages [number of delay stages] each having at least two paths [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2];

c. feeding back the propagated signal [F2] to the an input of the first circuit [11] path and to said phase detector [14][fig.1, 7];

d. detecting a phase difference [it is inherent to phase comparator] for producing signals [En1~Enn] for input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1].

41. As to claim 44, Ono teaches locked loop [digital phase-locked loop] comprising:

a. propagating a signal through a first circuit path [via load cap. Control 12, fig. 1, 2] having a stepwise variable [adder/subtracter circuit increments or decrements] capacitive load [load capacitance] [col. 4, lines 11 – 21];

b. propagating a signal through a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having a variable amount of drive associated therewith [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2];

c. feeding back the propagated signal [F2] to the an input of the first circuit [11] path and to said phase detector [14][fig.1, 7];

d. detecting a phase difference [it is inherent to phase comparator] for producing signals [En1~Enn] for input to said control circuit [15] for first and second circuit path [col. 4, lines 8 – 13, fig. 1].

42. As to claim 45, Ono teaches locked loop [digital phase-locked loop] comprising:

a. propagating a signal through a first circuit path [via load cap. Control 12, fig. 1, 2] having a variable amount [adder/subtracter circuit increments or decrements] of drive [load capacitance] associated therewith [col. 4, lines 11 – 21];

b. propagating a signal through a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least a fast [with less number of delay stages] and slow [with more number of delay stages] path [with

selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2];

c. feeding back the propagated signal [F2] to the an input of the first circuit [11] path and to said phase detector [14][fig.1, 7];

d. detecting a phase difference [it is inherent to phase comparator] for producing signals [En1~Enn] for input to said control circuit [15] for first and second circuit path [col. 4, lines 8 – 13, fig. 1].

43. As to claim 46, Ono teaches digital phase-locked loop [DLL] circuit and method of operation comprising:

a. propagating a signal [F1] through a first locked loop [DLL with phase comparator] to establish a phase relationship [inherent to phase comparator] between an output [F2, DPLL output clock signal] and reference signal [F1, reference clock signal][fig. 1];

b. propagating said signal [F1] through two different types of variable delay circuits, one circuit being substantially independent of process, temperature and voltage [PVT] variations [changes] [it is inherent property of Ono's first circuit path [via load cap control] with phase comparator to have substantially independent of process, temperature and voltage [PVT] variations as phase variation is independent of PVT variations] and one [second] circuit tracking changes in process, temperature and voltage [PVT] variations [changes] [Ono's second circuit path [variable delay stage control] with frequency comparator to have substantially tracks changes in PVT as frequency variation is dependent of PVT variations];

c. feeding back the propagated signal [F2] to the input of the first locked loop [DLL] and phase comparator [14]; and

d. detecting a phase difference [by comparing phase] between said feedback signal [F2] and a reference signal [F1, reference clock signal][fig. 1] to produce a control signal [phase compensation signal] for delay circuits [16, variable delay circuit][col. 4, lines 8 – 24][fig. 1, 2, 7, 8].

44. As to claim 47, Ono teaches digital phase-locked loop circuit and method of operation comprising:

a. propagating a signal [F1] through a first locked loop [DLL with phase comparator] to establish a phase relationship [inherent to phase comparator] between an output [F2, DPLL output clock signal] and reference signal [F1, reference clock signal][fig. 1];

b. propagating said signal [F1] through two different types [load cap. Control, delay stage control] of variable delay circuits [16 variable delay circuits], one circuit have a small intrinsic delay and the other circuit having a larger intrinsic delay [Ono's first circuit path with increment/decrement of load capacitance of having inherently a smaller intrinsic delay than the second circuit path with number of delay stages];

c. feeding back the propagated signal [F2] to the input of the first locked loop [DLL] and phase comparator [14]; and

d. detecting a phase difference [by comparing phase] between said feedback signal [F2] and a reference signal [F1, reference clock signal][fig. 1] to produce a control signal

[phase compensation signal] for delay circuits [16, variable delay circuit][col. 4, lines 8 – 24][fig. 1, 2, 7, 8].

45. As to claim 48, Ono teaches digital phase-locked loop circuit and method of operation comprising:

a. propagating a signal [F1] through a first locked loop [DLL with phase comparator] to establish a phase relationship [inherent to phase comparator] between an output [F2, DPLL output clock signal] and reference signal [F1, reference clock signal][fig. 1];

b. propagating said signal [F1] through a first circuit path [via load cap. Control 12, fig. 1, 2] having a stepwise variable [adder/subtracter circuit increments or decrements] capacitive load [load capacitance] [col. 4, lines 11 – 21];

c. propagating said signal [F1] through a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least two paths [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2];

d. feeding back the propagated signal [F2] to the input of the first locked loop [DLL] and phase comparator [14]; and

e. detecting a phase difference [by comparing phase] between said feedback signal [F2] and a reference signal [F1, reference clock signal][fig. 1] to produce a control signal [phase compensation signal] for delay circuits [16, variable delay circuit][col. 4, lines 8 – 24][fig. 1, 2, 7, 8].

46. As to claim 49, Ono teaches digital phase-locked loop circuit and method of operation comprising:

a. propagating a signal [F1] through a first locked loop [DLL with phase comparator] to establish a phase relationship [inherent to phase comparator] between an output [F2, DPLL output clock signal] and reference signal [F1, reference clock signal][fig. 1];

b. propagating said signal [F1] through a first circuit path [via load cap. Control 12, fig. 1, 2] having a stepwise variable [adder/subtracter circuit increments or decrements] capacitive load [load capacitance] [col. 4, lines 11 – 21];

c. propagating said signal [F1] through a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having a variable amount of drive [number of inverters, fig. 8] associated therewith [col. 10, lines 37 – 51, col. 4, lines 19 – 24, fig.2, 8];

d. feeding back the propagated signal [F2] to the input of the first locked loop [DLL] and phase comparator [14]; and

e. detecting a phase difference [by comparing phase] between said feedback signal [F2] and a reference signal [F1, reference clock signal][fig. 1] to produce a control signal [phase compensation signal] for delay circuits [16, variable delay circuit][col. 4, lines 8 – 24][fig. 1, 2, 7, 8].

47. As to claim 50, Ono teaches digital phase-locked loop circuit and method of operation comprising:

a. propagating a signal [F1] through a first locked loop [DLL with phase comparator] to establish a phase relationship [inherent to phase comparator] between an output [F2, DPLL output clock signal] and reference signal [F1, reference clock signal][fig. 1];

b. propagating said signal [F1] through a first circuit path [via load cap. Control 12, fig. 1, 2] having plurality of stages [adder/subtracter inherently represents plurality of stages] each having a variable amount of drive [variable load capacitance] associated therewith [col. 4, 57 – 60, fig. 1, 2];

c. propagating said signal [F1] through a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least a fast [with less number of delay stages] and slow [with more number of delay stages] path [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2];

d. feeding back the propagated signal [F2] to the input of the first locked loop [DLL] and phase comparator [14]; and

e. detecting a phase difference [by comparing phase] between said feedback signal [F2] and a reference signal [F1, reference clock signal][fig. 1] to produce a control signal [phase compensation signal] for delay circuits [16, variable delay circuit][col. 4, lines 8 – 24][fig. 1, 2, 7, 8].

Claim Rejections - 35 USC § 103

48. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

49. Claims 21 – 25, and 26 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker et al. [hereinafter as Baker], US Patent 6, 445, 231 [cited by applicant in IDS paper filed on 02/19/04], and further in view of Andresen, US Patent 5,808,478 [cited by applicant in IDS paper filed on 02/19/04].

50. Claims 21 – 25, are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker et al. [hereinafter as Baker], US Patent 6,445,231, and further in view of Andresen, US Patent 5,808,478.

51. As to claims 21, Baker discloses an invention and method for digital dual-loop DLL design [fig. 2A] with a first locked loop [205a, COARSE LOOP] for establishing a first phase relationship between an output signal [CLKout] and a reference signal [CLKin]; and a second locked loop [205b, FINE LOOP] responsive to the first locked loop [205a] and configured to establish a second phase relationship between the output signal [CLKout] and reference signal [CLKin], wherein a second locked loop comprises an interleaved delay line [DELAY LINE, fig. 12] generating an output signal [CLKout][fig. 11 – 12, and 14].

However, Baker does not disclose a delay line having two different types of delay circuits where the first is independent of process, temperature, and voltage [PVT] variation and the second is tracking changes in process, temperature and voltage variation. In summary, Backer does not teach chain of delay circuits wherein the first is independent of PVT variation and the second is dependent on PVT variation.

Andresen teaches a system and method for a digitally controlled output buffer with an interleaved delay line with a first portion [40, variable delay] providing a variable amount of delay substantially independent of [does not vary with] process, temperature, and voltage variations [col. 3, lines 59 – 62]; and a second portion [38, intrinsic delay] in series with said first portion and providing a variable amount of delay that substantially tracks [operable to account for] changes [variations] in process, temperature, and voltage [PVT] variations [col. 3, lines 26 - 29, fig. 2]. Andersen discloses to provide a compensated delay between an input and output of logic transition [col. 2, lines 1 – 9], and to vary drive as a function of load such that the slew rate can be made capacitive load independent [col. 2, lines 29 – 34], and also drive level varied without the use of current sources to vary the drive provided to the load [col. 2, lines 34 – 37, col. 3, lines 40 – 45].

It would have been an obvious to one of ordinary skill in art at the time of invention to combine the teachings of Baker with Andersen as both are related to adjustment/control of delay and Andersen's interleaved delay line with a first portion [40, variable delay] providing a variable amount of delay substantially independent of [does not vary with] process, temperature, and voltage variations [col. 3, lines 59 – 62]; and a second portion [38, intrinsic delay] in series with said first portion and providing a variable amount of delay that substantially tracks [operable to account for] changes [variations] in process, temperature, and voltage [PVT] variations will effectively vary slew rate such that, when capacitive load is increased, a lower impedance is presented to drive more current into load and, when capacitive load is decreased, the driving impedance is increased to drive less current into load [col. 3, lines 40 – 45].

52. As to claim 22, Baker teaches a first portion [205a] providing a variable amount of delay [wide frequency range] with little intrinsic [PVT dependent] delay and a second portion [205b] providing a variable amount of delay [delay range] with larger intrinsic [PVT dependent] delay [it is an inherent property of PVT independent coarse loop to have a small intrinsic (PVT dependent) delay than PVT dependent fine loop][col. 4, lines 17 – 20].

53. As to claim 23, Baker discloses to vary delay of first portion [205a] of delay line [111] by varying the load [number of stages] [col. 6, lines 20 – 28] and second portion [205b] of delay line [111] by selecting a desired signal path [col. 8, lines 34 – 50, fig. 10].

54. As to claim 24, Baker discloses the desired [selected] path signal is one of a slow [longer] path and a fast [shorter] path [col. 8, lines 39 –50, fig. 10].

55. As to claim 25, Baker discloses the desired [selected] path signal is one of a series path through an inverter or a parallel path through inverter [col. 8, lines 34 – 45, fig. 10].

56. As to claims 26, Baker discloses an invention and method for digital dual-loop DLL design [fig. 2A] with a first locked loop [205a, COARSE LOOP] for establishing a first phase relationship between an output signal [CLKout] and a reference signal [CLKin]; and a second locked loop [205b, FINE LOOP] responsive to the first locked loop [205a] and configured to establish a second phase relationship between the output signal [CLKout] and reference signal [CLKin], wherein a second locked loop comprises an interleaved delay line [DELAY LINE, fig. 12] generating an output signal [CLKout][fig. 11 – 12, and 14].

However, Baker does not disclose about an delay line having a first portion with a smaller intrinsic delay, and second portion with larger intrinsic value and producing control signals to control the delay. In summary, Backer does not teach chain of delay with a first

portion with smaller and, a second portion with larger intrinsic delay value and producing control signals to control the delay.

Andresen teaches system and method for digitally controlled output buffer with interleaved delay line with a first portion [112] providing a variable amount of delay with little intrinsic delay; a second portion [114] providing a variable amount of delay with larger intrinsic delay [fig. 5, 6], and generating control signal to control the delays of both portions [col. 3, lines 24 – 36, and 58 – 62]. Andersen discloses to provide a compensated delay between an input and output of logic transition [col. 2, lines 1 – 9], and to vary drive as a function of load such that the slew rate can be made capacitive load independent [col. 2, lines 29 – 34], and also drive level varied without the use of current sources to vary the drive provided to the load [col. 2, lines 34 – 37, col. 3, lines 40 – 45].

It would have been an obvious to one of an ordinary skill in art at the time of invention to combine teachings of Baker with Andersen as both are related to adjustment/control of delay and Andersen's interleaved delay line with a first portion [112] providing a variable amount of delay with little intrinsic delay; a second portion [114] providing a variable amount of delay with larger intrinsic delay [fig. 5, 6] will effectively vary slew rate such that, when capacitive load is increased, a lower impedance is presented to drive more current into load and, when capacitive load is decreased, the driving impedance is increased to drive less current into load [col. 3, lines 41 – 45].

57. As to claims 21, Baker discloses an invention and method for digital dual-loop DLL design [fig. 2A] with a first locked loop [205a, COARSE LOOP] for establishing a first phase relationship between an output signal [CLKout] and a reference signal [CLKin]; and a second

locked loop [205b, FINE LOOP] responsive to the first locked loop [205a] and configured to establish a second phase relationship between the output signal [CLKout] and reference signal [CLKin], wherein a second locked loop comprises an interleaved delay line [DELAY LINE, fig. 12] generating an output signal [CLKout][fig. 11 – 12, and 14].

However, Baker does not disclose about an delay line having two different types of delay circuits with first is independent of process, temperature, and voltage [PVT] variation and second is tracking changes in process, temperature and voltage variation. In summary, Backer does not teach chain of delay circuits wherein first independent of PVT variation and second is dependent on independent of PVT variation.

Andresen teaches system and method for digitally controlled output buffer with interleaved delay line with a first portion [40, variable delay] providing a variable amount of delay substantially independent of [does not vary with] process, temperature, and voltage variations [col. 3, lines 59 – 62]; and a second portion [38, intrinsic delay] in series with said first portion and providing a variable amount of delay that substantially tracks [operable to account for] changes [variations] in process, temperature, and voltage [PVT] variations [col. 3, lines 26 - 29, fig. 2].

It would have been an obvious to one of ordinary skill in art at the time of invention to combine teachings of Baker with Andersen as both are related to adjustment/control of delay and Andersen's interleaved delay line with a first portion [40, variable delay] providing a variable amount of delay substantially independent of [does not vary with] process, temperature, and voltage variations [col. 3, lines 59 – 62]; and a second portion [38, intrinsic delay] in series with said first portion and providing a variable amount of delay that substantially tracks [operable to

account for] changes [variations] in process, temperature, and voltage [PVT] variations will effectively vary slew rate such that, when capacitive load is increased, a lower impedance is presented to drive more current into load and, when capacitive load is decreased, the driving impedance is increased to drive less current into load [col. 3, lines 45].

58. As to claim 28, Baker discloses to vary delay of first portion [205a] of delay line [111] by varying the load [number of stages] [col. 6, lines 20 – 28] and second portion [205b] of delay line [111] by selecting a desired signal path [col. 8, lines 34 – 50, fig. 10].

59. As to claim 29, Baker discloses the desired [selected] path signal is one of a slow [longer] path and a fast [shorter] path [col. 8, lines 39 –50, fig. 10].

60. As to claim 30, Baker discloses the desired [selected] path signal is one of a series path through an inverter or a parallel path through inverter [col. 8, lines 34 – 45, fig. 10].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 703-305-3994. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Brown can be reached on 703-308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
June 14, 2004

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